Amendments to the Claims:

The following claims will replace all prior versions of the claims in this application (in the unlikely event that no claims follow herein, the previously pending claims will remain):

1. (Currently Amended) A receiver of a CDMA system employing a multiple access interference (MAI) cancellation apparatus, comprising:

the MAI cancellation apparatus ~~includes~~ comprising:

demodulating means for receiving a residual signal or a received signal from a calling terminal as a baseband spread signal on an over-sample basis and down-sampling the baseband spread signal ~~on~~ from the over-sample basis to a chip basis to thereby output a demodulation signal;

regenerating means for performing a bit decision for the demodulation signal, regenerating signals through the channelization and scrambling, and converting the regenerated signals to signals on the over-sample basis and the chip basis;

adding means for summing up the signals on the over-sample basis;

pulse shaping filtering means for filtering the summed-up signal to thereby output a band spread signal;

subtracting means for receiving the received signal and ~~for~~ subtracting the band spread signal from the received signal to thereby output the residual signal; and

delay means for keeping timing with the residual signal by delaying, on the chip basis, the signals ~~on the chip basis~~ outputted from the regenerating means,

wherein the MAI cancellation apparatus generates the demodulation signal by summing up the residual signal down-sampled on the chip basis at the demodulating means and the signals on the chip basis outputted from the delay means.

2. (Original) The receiver of the CDMA system as recited in claim 1, wherein the MAI cancellation apparatus further includes buffering means for storing the received signal and outputting the stored signal to the subtracting means.

3. (Currently Amended) The receiver of the CDMA system as recited in claim 2 comprising:

a plurality of MAI cancellation apparatuses,

wherein a succeeding MAI cancellation apparatus receives as input signals a residual signal outputted from a subtracting means, a signal on the chip basis outputted from

a delay means and a the received signal outputted from a buffering means of a previous MAI cancellation apparatus.

4. (Currently Amended) The receiver of the CDMA system as recited in claim 2, wherein, in the MAI cancellation apparatus, the residual signal outputted from the subtracting means is inputted to the demodulating means and the delayed signals on the chip basis outputted from the delay means are fed back to the demodulating means.

5. (Original) The receiver of the CDMA system as recited in claim 1, wherein the demodulating means contains demodulators as many as the number of users of the CDMA system and the regenerating means has regenerators as many as the number of users of the CDMA system.

6. (Currently Amended) The receiver of the CDMA system as recited in claim 5, wherein the demodulator has:

I signal/Q signal decimators for down-sampling an I channel signal and a Q channel signal of the received signal or the residual signal, outputted from the subtracting means, to signals on the chip basis, respectively;

a dedicated physical data channel (DPDCH) demodulator for demodulating a data signal from a signal outputted from the I signal decimator;

a dedicated physical control channel (DPCCH) demodulator for demodulating a control signal from a signal outputted from the Q signal decimator;

a channel estimator for outputting a channel estimation value per path from a pilot signal outputted from the DPCCH demodulator;

a DPDCH maximum ratio combiner for receiving the demodulated data signal and the channel estimation value per path and outputting a maximum ratio combination bit decision value of a dedicated physical data channel bit; and

a DPCCH maximum ratio combiner for receiving the demodulated control signal and the channel estimation value per path and outputting a maximum ratio combination bit decision value of a dedicated physical control channel bit.

7. (Original) The receiver of the CDMA system as recited in claim 6, wherein the demodulator has I signal/Q signal decimators, DPDCH demodulators, DPCCH demodulators and channel estimators as many as the number of multi-paths of each user.

8. (Original) The receiver of the CDMA system as recited in claim 7, wherein the regenerator has:

DPDCH bit deciding means for receiving the maximum ratio combination bit decision value of the dedicated physical data channel bit and performing a bit decision;

DPCCH bit deciding means for receiving the maximum ratio combination bit decision value of the dedicated physical control channel bit and executing a bit decision;

channelization means for spreading the decision values of the DPDCH bit deciding means and the DPCCH bit deciding means by using a unique spread code per channel;

channel estimation multiplier for outputting a dedicated physical data channel regeneration signal and a dedicated physical control channel regeneration signal by multiplying the channel estimation value with the spread signal outputted form the channelization means;

scrambling means for an I signal and a Q signal on the chip basis by multiplying the dedicated physical data channel regeneration signal and the dedicated physical control channel regeneration signal with a scramble code for sorting users;

zero inserting means for converting the I signal and the Q signal to signals on the over-sample basis and outputting the converted signals; and

path selecting means for outputting the I signal and the Q signal on the over-sample basis to the adding means and providing the I signal and the Q signal on the chip basis to the delay means.

9. (Original) The receiver of the CDMA system as recited in claim 8, wherein the zero inserting means converts the I signal and the Q signal on the chip basis to the signals on the over-sample basis by inserting (the number of over-samples -1) number of zeros to the I signal and the Q signal on the chip basis.

10. (Original) The receiver of the CDMA system as recited in claim 8, wherein the DPDCH bit deciding means performs the bit decision by setting as 1 if the maximum ratio combination bit decision value of the dedicated physical data channel bit is not a negative number and performing a bit decision and -1 if otherwise and the DPCCH bit deciding means executes the bit decision by determining as 1 if the maximum ratio combination bit decision value of the dedicated physical control channel bit is not a negative number and -1 if otherwise.